2631
IFW

Attorney Docket No. Q01-1009-US1 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Aliahmad et al.
Serial No. 09/870,704
Filed: June 1, 2001
For: TIMING SKEW COMPENSATION TECHNIQUE FOR PARALLEL DATA CHANNELS

Group Art Unit: 2631
Examiner: Wang

Date: November 5, 2004

Mail Stop Amendment
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

INTERVIEW SUMMARY

Sir:

Applicants provide the present Interview Summary in response to an Examiner initiated telephone interview on November 4, 2004.

Applicants appreciate the Examiner's indication in the telephone interview that the pending claims are allowable once Claims 1 and 31 are amended to provide proper antecedent basis for certain recitations. In the interview, it was agreed that Claims 1 and 31 would be amended as shown below through an Examiner's Amendment to place all of the pending claims in condition for allowance.

Claim 1. (Currently amended) An apparatus for detecting and correcting the timing skew of a data signal in a parallel data transmission system, comprising:

a data path for adjusting the timing skew of the data signal with respect to a clock signal, said data path including: a delay digital-to-analog converter (DAC), a falling edge DAC, at least two receive registers, an output multiplexer, and control logic;

a clock path for correcting the duty-cycle of a receive clock and for delaying said receive clock in normal receive operations, wherein said clock path is selectably switchable between a timing skew correction mode and a receive-data mode;

a local accurate tuning system for generating a tuning signal to tune all of the delay elements of said parallel data transmission system according to ~~said~~ a bit-cell time of the data signal; and

wherein said control logic detects the timing skew of the data signal and controls said delay DAC and said falling edge DAC to provide appropriate delay to the data signal in accordance with the detected timing skew of said data signal.

Claim 31. (Currently amended) A method for detecting and correcting the timing skew of data in a parallel data transmission system having a receive clock and at least one data signal with a bit-cell time, the method comprising:

generating a tuning signal having an amplitude based on a local accurate clock;

correcting the duty-cycle of the receive clock according to said tuning signal and the bit-cell time;

determining the time delay of said at least one data signal relative to the receive clock and said tuning signal;

adjusting the time delay of said at least one data signal relating to the receive clock;

adjusting the time delay of falling edges of said at least one data signal relative to said receive clock;

capturing data from said at least one data signal on the rising and falling edges of said receive clock; and

swapping the outputs of ~~the~~ at least two receive registers used in said capturing if the detected time-skew of said at least one data signal reaches a predetermined level.

In light of the above amendments and remarks, Applicants respectfully submit that all of the pending claims are now in condition for allowance.

Respectfully submitted,

David K. Purks
Registration No. 40,133
Attorney for Applicants

USPTO Customer No. 20792
Myers Bigel Sibley & Sajovec, P.A.
Post Office Box 37428
Raleigh, NC 27627
Telephone: (919) 854-1400
Facsimile: (919) 854-1401

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on November 5, 2004.

Audra Wooten